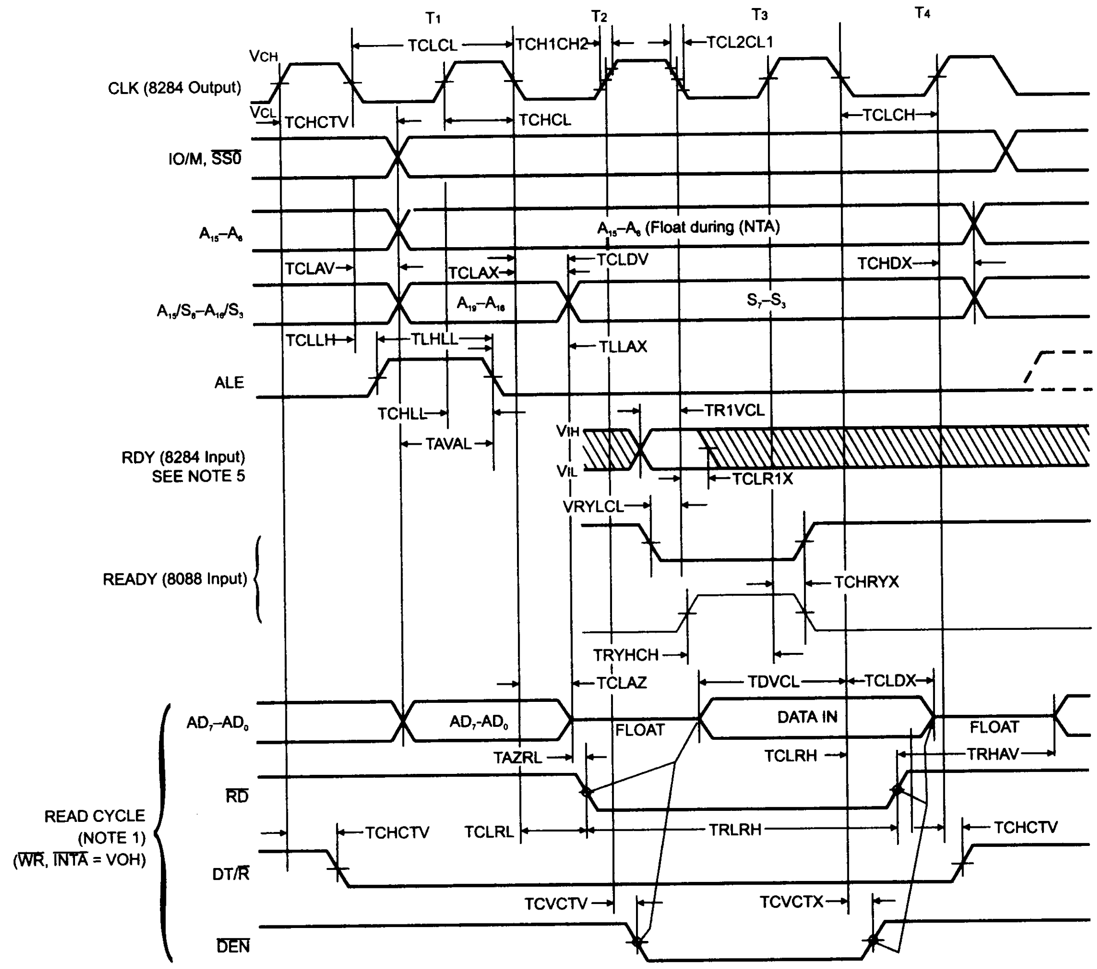


FIGURE 8–11 Minimum mode 8088 bus timing for a read operation.

In T4, all bus signals are deactivated in preparation for the next bus cycle. This is also the time when the 8086/8088 samples the data bus connections for data that are read from memory or I/O. In addition, at this point, the trailing edge of the WR signal transfers data to the memory or I/O, which activates and writes when the WR signal returns to a logic 1 level.

Read Timing

Figure 8–11 also depicts the read timing for the 8088 microprocessor. The 8086 read timing is identical except that the 8086 has 16 rather than eight data bus bits. A close look at this timing diagram should allow you to identify all the main events described for each T state.

The most important item contained in the read timing diagram is the amount of time allowed the memory or I/O to read the data. Memory is chosen by its access time, which is the fixed amount of time that the microprocessor allows it to access data for the read operation. It is therefore extremely important that the memory chosen complies with the limitations of the system.

A.C. CHARACTERISTICS (8088: T_A = 0°C to 70°C, Vcc = 5V ± 10%)°
(8088-2: T_A = 0°C to 70°C, Vcc = 5V ± 5%)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period	200	300	125	500	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLOX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	118		68		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY inactive to CLK (See Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLAV	Address Valid Delay	10	110	10	60	ns	C_L = 20-100 pF for all 8088 Outputs in addition to internal loads
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After $\overline{\text{WR}}$	TCLCH−30		TCLCH−30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{\text{RD}}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{\text{RD}}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{\text{RD}}$ Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{\text{RD}}$ Width	2TCLCL−75		2TCLCL−50		ns	
TWLWH	$\overline{\text{WR}}$ Width	2TCLCL−60		2TCLCL−40		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−40		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

FIGURE 8–12 8088 AC characteristics.

The microprocessor timing diagram does not provide a listing for memory access time. Instead, it is necessary to combine several times to arrive at the access time. To find memory access time in this diagram, first locate the point in T3 when data are sampled. If you examine the timing diagram closely, you will notice a line that extends from the end of T3 down to the data bus. At the end of T3, the microprocessor samples the data bus.

Memory access time starts when the address appears on the memory address bus and continues until the microprocessor samples the memory data at T3. Approximately three T states elapse between these times. (See Figure 8–12 for the following times.) The address does not appear until T_{CLAV} time (110 ns if the clock is 5 MHz) after the start of T1. This means that T_{CLAV} time must be subtracted from the three clocking states (600 ns) that separate the appearance of the address (T1) and the sampling of the data (T3). One other time must also be subtracted: the data setup time (T_{DVCL}), which occurs before T3. Memory access time is thus three clocking states minus the sum of T_{CLAV} and T_{DVCL}. Because T_{DVCL} is 30 ns with a 5 MHz clock, the allowed memory access time is only 460 ns (access time = 600 ns – 110 ns – 30 ns).

The memory devices chosen for connection to the 8086/8088 operating at 5 MHz must be able to access data in less than 460 ns, because of the time delay introduced by the address decoders and buffers in the system. At least a 30- or 40-ns margin should exist for the operation of these circuits. Therefore, the memory speed should be no slower than about 420 ns to operate correctly with the 8086/8088 microprocessors.

The only other timing factor that may affect memory operation is the width of the RD strobe. On the timing diagram, the read strobe is given as T_{RLRH}. The time for this strobe is 325 ns (5 MHz clock rate), which is wide enough for almost all memory devices manufactured with an access time of 400 ns or less.

Write Timing

Figure 8–13 illustrates the write-timing diagram for the 8088 microprocessor. (Again, the 8086 is nearly identical, so it need not be presented here in a separate timing diagram.)

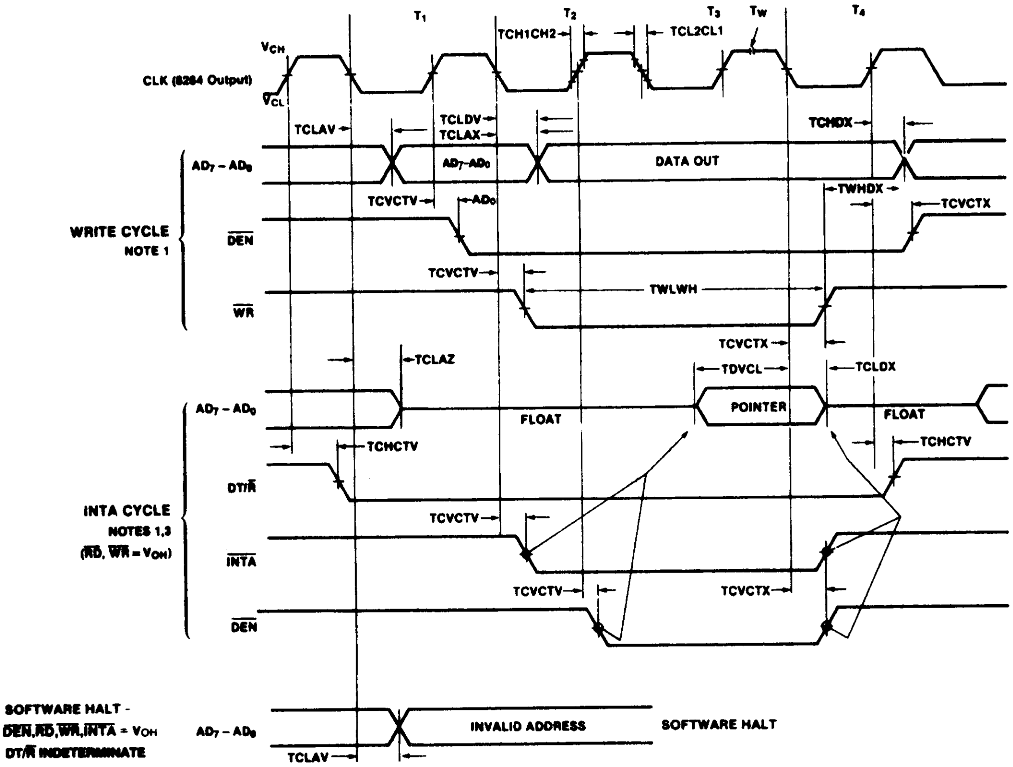
The main differences between read and write timing are minimal. The RD strobe is replaced by the WR strobe, the data bus contains information for the memory rather than information from the memory, and DT/R remains a logic 1 instead of a logic 0 throughout the bus cycle.

When interfacing some memory devices, timing may be especially critical between the point at which WR becomes a logic 1 and the time when the data are removed from the data bus. This is the case because, as you will recall, memory data are written at the trailing edge of the WR strobe. According to the timing diagram, this critical period is T_{WHDX} or 88 ns when the 8088 is operated with a 5 MHz clock. Hold time is often much less than this; it is, in fact, often 0 ns for memory devices. The width of the WR strobe is T_{WLWH} or 340 ns at a 5 MHz clock rate. This rate is compatible with most memory devices that have an access time of 400 ns or less.

8–5 READY AND THE WAIT STATE

As we mentioned earlier in this chapter, the READY input causes wait states for slower memory and I/O components. A **wait state** (T_W) is an extra clocking period, inserted between T2 and T3, to lengthen the bus cycle. If one wait state is inserted, then the memory access time, normally 460 ns with a 5 MHz clock, is lengthened by one clocking period (200 ns) to 660 ns.

In this section, we discuss the READY synchronization circuitry inside the 8284A clock generator, show how to insert one or more wait states selectively into the bus cycle, and examine the READY input and the synchronization times it requires.



NOTES:

1. ALL SIGNALS SWITCH BETWEEN Y_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8086 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

FIGURE 8–13 Minimum mode 8088 write bus timing.

The READY Input

The READY input is sampled at the end of T2 and again, if applicable, in the middle of T_W. If READY is a logic 0 at the end of T2, T3 is delayed and T_W is inserted between T2 and T3. READY is next sampled at the middle of T_W to determine whether the next state is T_W or T3. It is tested for a logic 0 on the 1-to-0 transition of the clock at the end of T2, and for a 1 on the 0-to-1 transition of the clock in the middle of T_W.

The READY input to the 8086/8088 has some stringent timing requirements. The timing diagram in Figure 8–14 shows READY causing one wait state (T_W), along with the required setup and hold times from the system clock. The timing requirement for this operation is met by the internal READY synchronization circuitry of the 8284 A clock generator. When the 8284A is used for READY, the RDY (ready input to the 8284A) input occurs at the end of each T state.

RDY and the 8284A

RDY is the synchronized ready input to the 8284A clock generator. The timing diagram for this input is provided in Figure 8–15. Although it differs from the timing for the READY input to the 8086/8088, the in-

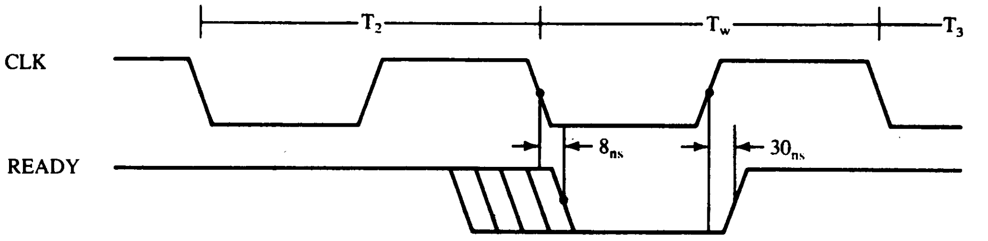


FIGURE 8–14 8086/8088 READY input timing.

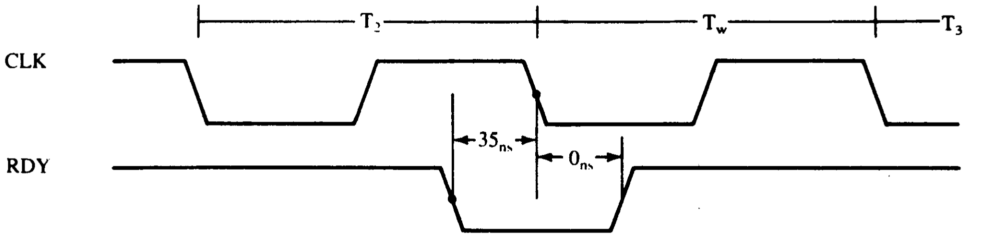


FIGURE 8–15 8284A RDY input timing.

ternal 8284A circuitry guarantees the accuracy of the READY synchronization provided to the 8086/8088 microprocessors.

Figure 8–16 again depicts the internal structure of the 8284A. The bottom half of this diagram is the READY synchronization circuitry. At the leftmost side, the RDY1 and AEN1 inputs are ANDed, as are the RDY2 and AEN2 inputs. The outputs of the AND gates are then ORed to generate the input to the one or two stages of synchronization. In order to obtain a logic 1 at the inputs to the filp-flops, RDY1 ANDed with AEN1 must be active or RDY2 ANDed with AEN2 must be active.

The ASYNC input selects one stage of synchronization when it is a logic 1 and two stages when it is a logic 0. If one stage is selected, then the RDY signal is kept from reaching the 8086/8088 READY pin until the next negative edge of the clock. If two stages are selected, the first positive edge of the clock captures RDY in the first flip-flop. The output of this flip-flop is fed to the second flip-flop, so on the next negative edge of the clock, the second flip-flop captures RDY.

Figure 8–17 illustrates a circuit used to introduce almost any number of wait states for the 8086/8088 microprocessors. Here, an eight-bit serial shift register (74LS164) shifts a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A. With appropriate strapping, this circuit can provide various numbers of wait states. Notice also how the shift register is cleared back to its starting point. The output of the register is forced high when the RD, WR, and INTA pins are all logic 1s. These three signals are high until state T2, so the shift register shifts for the first time when the positive edge of the T2 arrives. If one wait is desired, output Q_B is connected to the OR gate. If two waits are desired, output Q_C is connected, and so forth.

Notice in Figure 8–17 that this circuit does not always generate wait states. It is enabled from the memory only for memory devices that require the insertion of waits. If the selection signal from a memory device is a logic 0, the device is selected; then this circuit will generate a wait state.

Figure 8–18 illustrates the timing diagram for this shift register wait state generator when it is wired to insert one wait state. The timing diagram also illustrates the internal contents of the shift register's flip-flops to present a more detailed view of its operation. In this example, one wait state is generated.

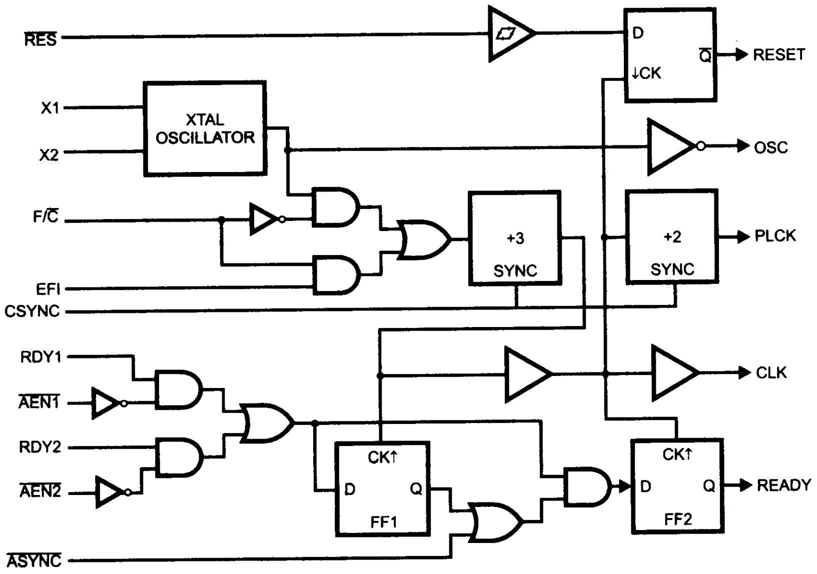


FIGURE 8–16 The internal block diagram of the 8284A clock generator. (Courtesy of Intel Corporation).

8–6 MINIMUM MODE VERSUS MAXIMUM MODE

There are two available modes of operation for the 8086/8088 microprocessors: minimum mode and maximum mode. Minimum mode operation is obtained by connecting the mode selection pin MN/MX to ±5.0 V, and maximum mode is selected by grounding this pin. Both modes enable different control structures for the 8086/8088 microprocessors. The mode of operation provided by minimum mode is similar to that of the 8085A, the most recent Intel eight-bit microprocessor. The maximum mode is unique and designed to be used whenever a coprocessor exists in a system. Note that the maximum mode was dropped from the Intel family, beginning with the 80286 microprocessor.

Minimum Mode Operation

Minimum mode operation is the least expensive way to operate the 8086/8088 microprocessors (see Figure 8–19 for the minimum mode 8088 system). It costs less because all the control signals for the memory and I/O are generated by the microprocessor. These control signals are identical to those of the Intel 8085A, an earlier eight-bit microprocessor. The minimum mode allows the 8085A, eight-bit peripherals to be used with the 8086/8088 without any special considerations.

Maximum Mode Operation

Maximum mode operation differs from minimum mode in that some of the control signals must be externally generated. This requires the addition of an external bus controller—the 8288 bus controller (see Figure 8–20 for the maximum mode 8088 system). There are not enough pins on the 8086/8088 for bus control during maximum mode because new pins and new features have replaced some of them. Maximum mode is used only when the system contains external coprocessors such as the 8087 arithmetic coprocessor.

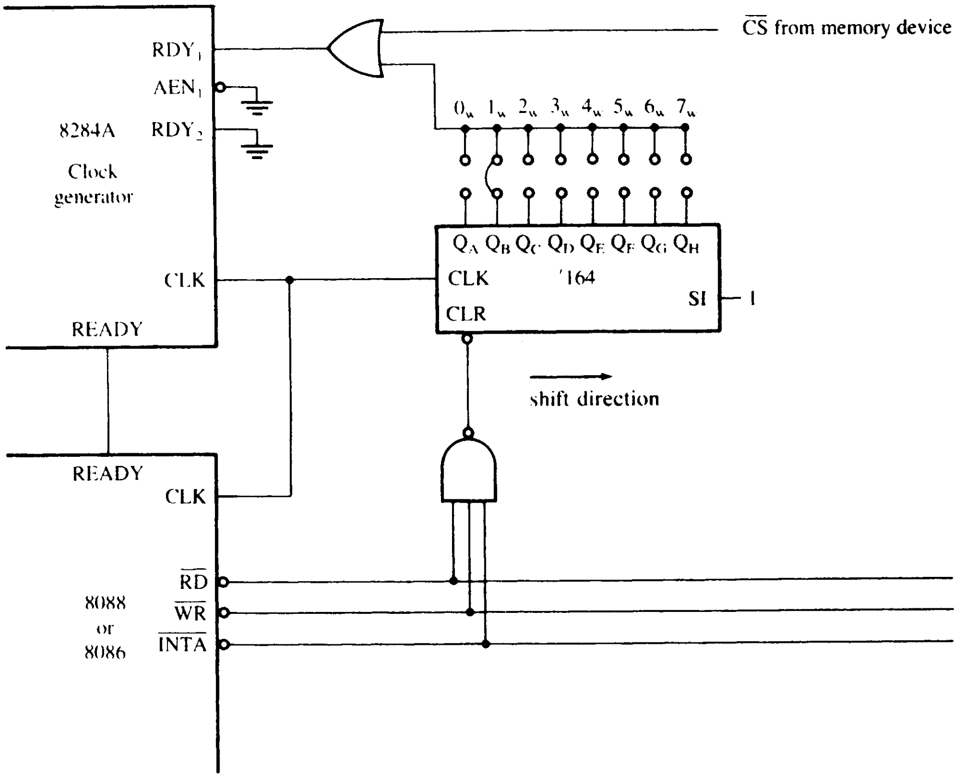


FIGURE 8–17 A circuit that will cause between 0 and 7 wait states.

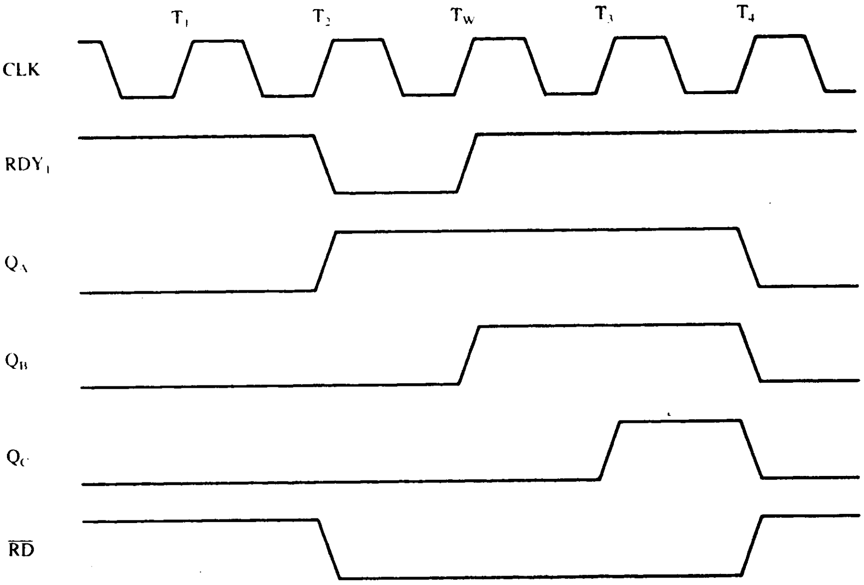


FIGURE 8–18 Wait state generation timing of the circuit of Figure 8–17.

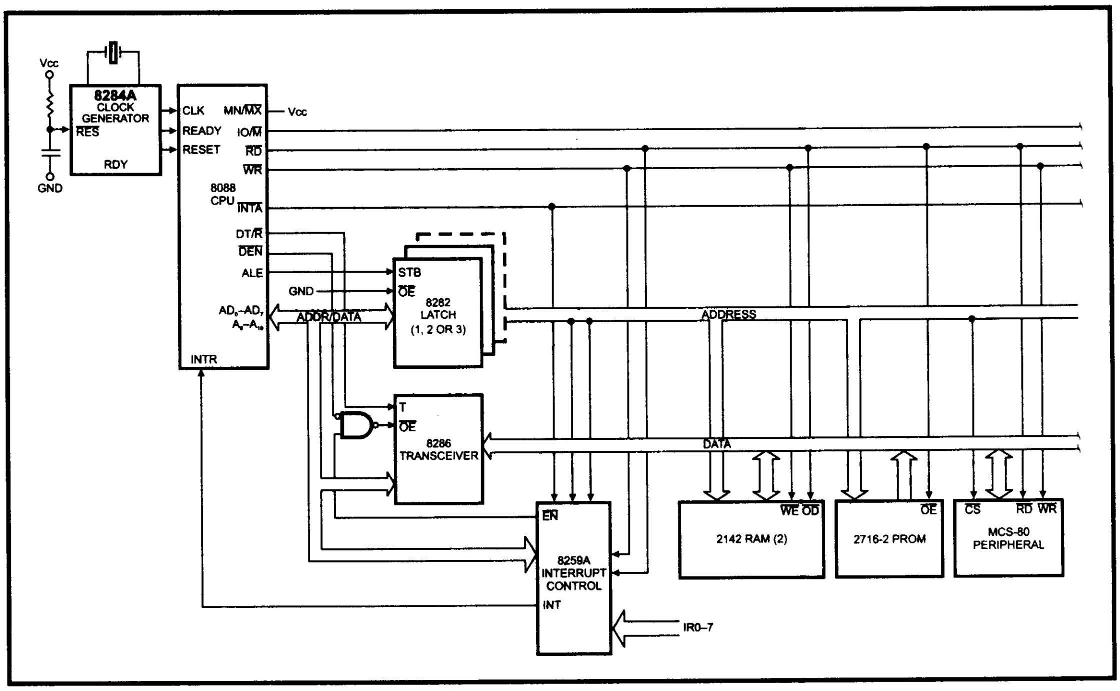


FIGURE 8–19 Minimum mode 8088 system.

The 8288 Bus Controller

An 8086/8088 system that is operated in maximum mode must have an 8288 bus controller to provide the signals eliminated from the 8086/8088 by the maximum mode operation. Figure 8–21 illustrates the block diagram and pin-out of the 8288 bus controller.

Notice that the control bus developed by the 8288 bus controller contains separate signals for I/O (IORC and IOWC) and memory (MRDC and MWTC). It also contains advanced memory (AMWC) and I/O (AIOWC) write strobes, and the INTA signal. These signals replace the minimum mode ALE, WR, IO/M, DT/R, DEN, and INTA, which are lost when the 8086/8088 microprocessors are operated in the maximum mode.

Pin Functions. The following list provides a description of each pin of the 8288 bus controller.

S2, S1, and S0 **Status** inputs are connected to the staus output pins on the 8086/8088 microprocessor. These three signals are decoded to generate the timing signals for the system.

CLK The **clock** input provides internal timing and must be connected to the CLK output pin of the 8284A clock generator.

ALE The **address latch enable** output is used to demultiplex the address/data bus.

DEN The **data bus enable** pin controls the bi-directional data bus buffers in the system. Note that this is an active high output pin that is the opposite polarity from the DEN signal found on the microprocessor when operated in the minimum mode.

DT/R The **data transmit/receive** signal is output by the 8288 to control the direction of the bi-directional data bus buffers.

AEN The **address enable** input causes the 8288 to enable the memory control signals.

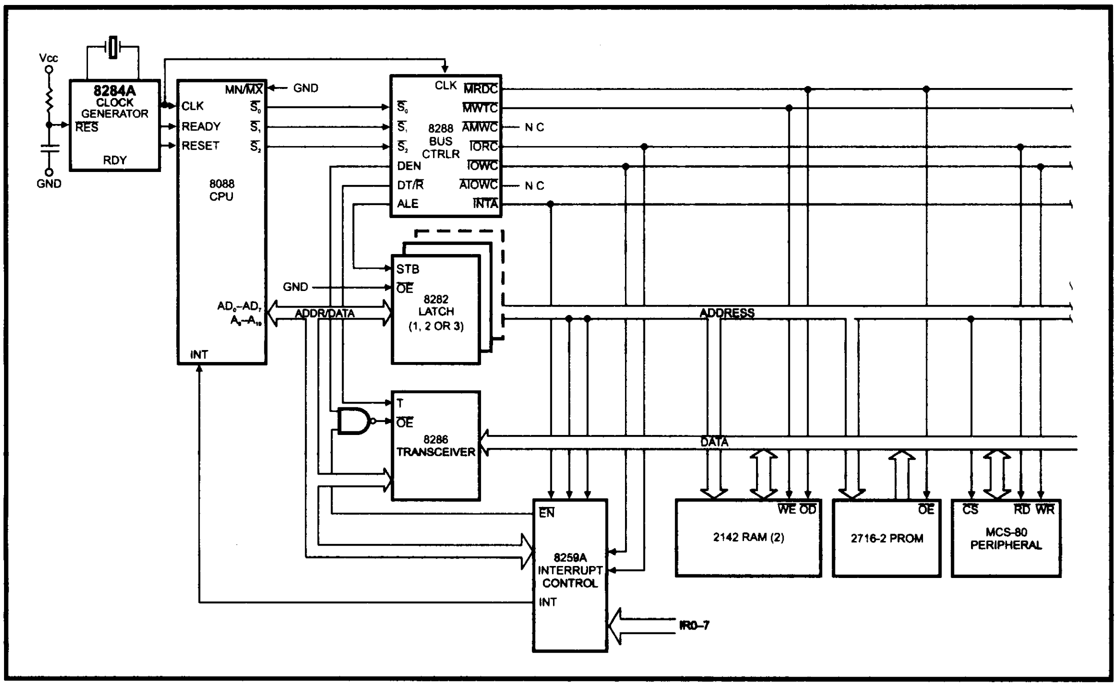


FIGURE 8–20 Maximum mode 8088 system.

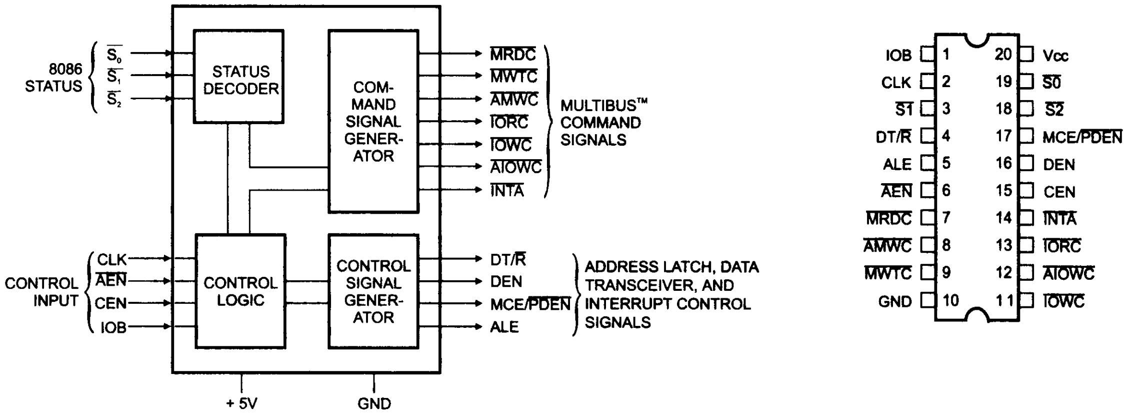


FIGURE 8–21 The 8288 bus controller: (a) block diagram and (b) pin-out.

CEN The **control enable** input enables the command output pins on the 8288.

IOB The **I/O bus mode** input selects either the I/O bus mode or system bus mode operation.

AIOWC The **advanced I/O write** is a command output used to provide I/O with an advanced I/O write control signal.

IOWC The **I/O write** command output provides I/O with its main write signal.

IORC The **I/O read** command output provides I/O with its read control signal.

AMWC The **advanced memory write** control pin provides memory with an early or advanced write signal.

MWTC The **memory write** control pin provides memory with its normal write control signal.

MRDC The **memory read** control pin provides memory with a read control signal.

INTA The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.

MCE/PDEN The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high

8–7 THE 80X87 ARCHITECTURE

The 80X87 is designed to operate concurrently with the microprocessor. The 80X87 executes 68 different instructions. The microprocessor executes all normal instructions and the 80X87 executes arithmetic coprocessor instructions. Both the microprocessor and coprocessor can execute their respective instructions simultaneously or concurrently. The numeric or arithmetic coprocessor is a special-purpose microprocessor that is especially designed to efficiently execute arithmetic and transcendental operations.

The microprocessor intercepts and executes the normal instruction set, and the coprocessor intercepts and executes only the coprocessor instructions. Recall that the coprocessor instructions are actually escape (ESC) instructions. These instructions are used by the microprocessor to generate a memory address for the coprocessor so that the coprocessor can execute a coprocessor instruction.

Internal Structure of the 80X87

Figure 8–22 shows the internal structure of the arithmetic coprocessor. Notice that this device is divided into two major sections: the control unit and the numeric execution unit.

The **control unit** interfaces the coprocessor to the microprocessor-system data bus. Both the devices monitor the instruction stream. If the instruction is an ESCape (coprocessor) instruction, the coprocessor executes it; if not, the microprocessor executes it.

The **numeric execution unit** (NEU) is responsible for executing all coprocessor instructions. The NEU has an eight-register stack that holds operands for arithmetic instructions and the results of arithmetic instructions. Instructions either address data in specific stack data-registers or use a push-and-pop mechanism to store and retrieve data on the top of the stack. Other registers in the NEU are status, control, tag, and exception pointers. A few instructions transfer data between the coprocessor and the AX register in the microprocessor. The FSTSW AX instruction is the only instruction available to the coprocessor that allows direct communications to the microprocessor through the AX register. Note that the 8087 does not contain the FSTSW AX instruction.

The stack within the coprocessor contains eight registers that are each 80 bits wide. These stack registers always contain an 80-bit extended-precision floating-point number. The only time that data appear as any other form is when they reside in the memory system. The coprocessor converts from signed integer, BCD, single-precision, or double-precision form as the data are moved between the memory and the coprocessor register stack.

Status Register. The status register (see Figure 8-23) reflects the overall operation of the coprocessor. The status register is accessed by executing the instruction (FSTSW), which stores the contents of the status register into a word of memory. Once status is stored in memory, the bit positions of the status register can be examined by normal software. Following is a list of the status bits and their applications: